Vector-Low-Density Parity-Check™ (V-LDPC™) Coding Solution Data Sheet

High Speed, High Performance Advanced Forward-Error Correction (FEC) Intellectual Property (IP) Cores

Overview

The Vector-LDPC™ Coding Solution consists of a scalable family of high-speed Low-Density Parity-Check (LDPC) encoders and decoders in the form of an intellectual property (IP) core that can be used in communication systems requiring Forward Error Correction (FEC). The code rate and design are programmable and changeable on-the-fly. The scalable architecture can support a wide range of throughputs (up to 10Gbps) and a variety of design requirements.

Vector-LDPC™ codes have been successfully implemented in Flarion's flash-OFDM™ system for mobile wireless communications system.

Low-density parity-check (LDPC) codes are a class of binary linear error-correcting codes that can be decoded by an iterative soft-in, soft-out (SISO) decoding algorithm. Flarion has developed a powerful architecture for LDPC codes, allowing for high-speed performance and programmable LDPC code designs, yielding significant advantages over Turbo Codes and other FEC implementations.

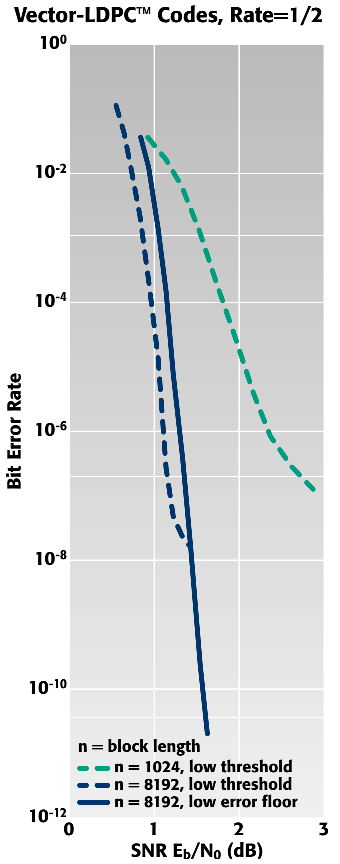
Vector-LDPC™ codes beat out Turbo Codes in performance, with less hardware complexity, higher throughput, more flexibility and lower error floors!

LDPC codes offer superior coding gain exceeding that of Turbo Codes. They can be designed to have very low error-floors, eliminating the need for an outer Reed-Solomon code. The Vector-LDPC™ solution supports fully programmable LDPC code designs, allowing customization for each application. Flarion's parallel architecture enables the efficient encoding and decoding of LDPC codes, making the Vector-LDPC™ solution well suited for high-speed applications.

Many high-speed communications applications stand to benefit from the large coding gains, high data rate, and smaller hardware size of these IP cores.

Applications

- Optical Fiber Communications
- Satellite (digital video and audio broadcast)
- Storage (magnetic, optical, holographic)
- Wireless (mobile, fixed)
- Wireline (cable modems, DSL)



Vector-LDPC™ Solution

- LDPC Encoder Core
- LDPC Decoder Core

Selected Features

- Efficient encoding algorithm
- Optimized LDPC code designs and minimal quantization loss yield near-capacity performance
- "Soft-in, soft-out" decoder compatible with turbo equalization
- Compatible with various modulation formats (QPSK, QAM)
- Early detection of convergence
- Improved average throughput due to statistical multiplexing buffers

Flexibility

- Highly parallel and scalable
- Supports a wide range of data speeds and hardware sizes
- Programmable coding rates and flexible block lengths
- Firmware allows downloading and fast swapping of LDPC codes
- LDPC codes are optimized for low error floors, large coding gains, high speed, etc.

Deliverables

- VHDL netlist
- VHDL test bench and test vectors
- Documentation
- C++ and MATLAB software models
- LDPC code designs
- Support and maintenance contract

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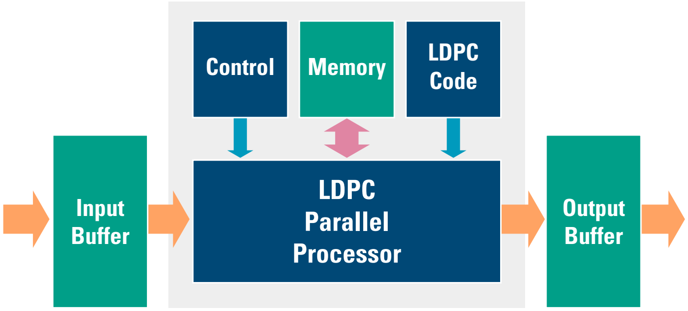
Vector-LDPC™ IP Core Architecture



The basic architecture for the **Vector-LDPC™ encoder and decoder cores** involves a custom-designed dedicated parallel processor that reads in a LDPC code description to perform parallel computations on the data stored in memory. In addition, the use of input and output buffers increases the average throughput through *statistical multiplexing*.

The decoder core implements a low complexity message-passing algorithm that closely approximates the best decoding algorithm (known as "belief propagation"). The decoder takes soft inputs that are quantized to up to 5 bits of precision.

The performance and complexity of this architecture can be estimated from the following key parameters:

- F_E and F_D are the clock frequencies of the encoder and decoder cores (e.g., 100 MHz for FPGA, >200MHz for ASIC)
- Z is the parallelism factor (typically 16, 32, 64 or 128)
- L is the codeword length (e.g., 1000 bits)
- R is the code rate (e.g., 1/2)
- N is the average number of decoding iterations (e.g., 20)

LDPC	User Data Rate	Memory	Gate Count
Encoder IP Core	$\frac{(F_E)(Z)(R)}{6}$ Mbps	10L bits	500(Z) gates
Decoder IP Core	$\frac{(F_D)(Z)(R)}{3(N)}$ Mbps	30L bits	2500(Z) gates

Estimates of the key metrics of the IP cores are shown in the table.

For an FPGA with F_E and F_D equal to $100MHz$, $Z=128$, $L=10K$ bits, $R=0.9$ and $N=10$, the estimated user data rate is **1.9Gbps** using 64K logic gates and 13KB memory for the encoder, and **384Mbps** using 320K gates and 38KB memory for the decoder.

For an ASIC with F_D equal to $325MHz$, $Z=1024$, $L=50K$ bits, $R=0.9$ and $N=10$, the decoder operates at **10Gbps** using roughly 2.6M gates and 190KB memory.

The throughput is determined by the *average* number of decoding iterations N, due to statistical multiplexing using the input/output buffers. Fewer iterations are needed for some situations (e.g., high code rate R, high SNR), leading to very high throughput.

The coding gain is determined by the LDPC code design, the code rate R, and the codeword length L. Lower rates and longer codewords lead to larger coding gain.

Vector-LDPC™ Codes Integrated in Mobile Broadband Wireless Chipset

Flarion Technologies has integrated Vector-Low-Density Parity Check™ (V-LDPC™) codes into its flash-OFDM™ mobile wireless chipsets for end-to-end Internet Protocol (IP)-based mobile broadband networks. This industry-leading forward error-correction (FEC) technology yields advantages in increased transmission distance and superior robustness over wireless channels.

The implementation occupies relatively small hardware area, as seen in the following table. "Device resources" refers to the number of logic blocks (CLBs) or logic gates that are occupied by the Vector-LDPC™ decoder core.

In this case, the LDPC encoder is simple enough to be implemented as DSP software. The supported modulation schemes include QPSK and 16QAM. The coding rates currently used include rates 1/6, 1/3, 1/2, 2/3 and 5/6. The data rate of 3Mbps is the maximum throughput currently used in the flash-OFDM™ system for a mobile device.

Version	Chip	Device Resources
flash-OFDM™ FPGA	Virtex-E	2500 CLBs
flash-OFDM™ ASIC	0.18µ ASIC	45K gates

More information about Vector-LDPC™ codes can be found at ***www.flarion.com/ldpc***

All interested parties are advised to contact Flarion Technologies at ***ldpc@flarion.com***

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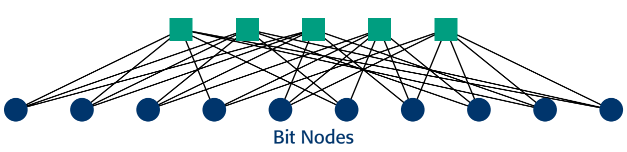
Background

In digital communications and storage systems, channel coding introduces redundancy into a data sequence to protect against errors introduced by the channel. The benefit is often characterized in terms of the energy savings for reliable delivery of information. This *coding gain* can be used in various ways: to increase the reach of a communications system; to reduce the required transmit power or spectrum; and to decrease the demands on the accuracy or fidelity of other system components.

Binary block codes represent a class of channel coding schemes that operate on a finite block of bits, such that the decoding occurs independently for each block. LDPC codes are a special class of binary block codes that can be decoded with an iterative soft-decision decoding algorithm called the message-passing algorithm (also known as “belief propagation”).

The message-passing decoding of LDPC codes involves simple computations executed in parallel. LDPC codes can be represented by Tanner graphs with two types of nodes. The *variable* nodes (“bit nodes”) correspond to elements of the codeword and the *constraint* nodes (“check nodes”) correspond to parity-check constraints that define the code. The decoding algorithm operates by exchanging messages back and forth along the edges of the graphs. Outgoing messages are computed based on the incoming messages to each node using simple computations. After multiple iterations, the decoder outputs the decoded codeword, which satisfies the parity-check matrix.

Graph representation of LDPC codes



Invented by Prof. Robert Gallager of MIT, LDPC codes have recently become a very active area of research, extending and improving on the work on Turbo Codes. By proper choice of the structure of the graph, LDPC codes can be constructed to perform better than Turbo Codes, setting the record for the highest achieved coding gain.

A leading pioneer and expert on the analysis and design of LDPC codes, **Tom Richardson** has led a design team at Flarion to develop an efficient hardware architecture suited to these powerful optimized LDPC codes. Incorporating the latest research innovations and using novel unpublished code constructions, Vector-LDPC™ codes are designed to maximize coding gain and optimize key parameters.

The Vector-LDPC™ architecture is an efficient, flexible, highly optimized, high-speed parallel implementation of a low-complexity message-passing algorithm that results in near-capacity performance.

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